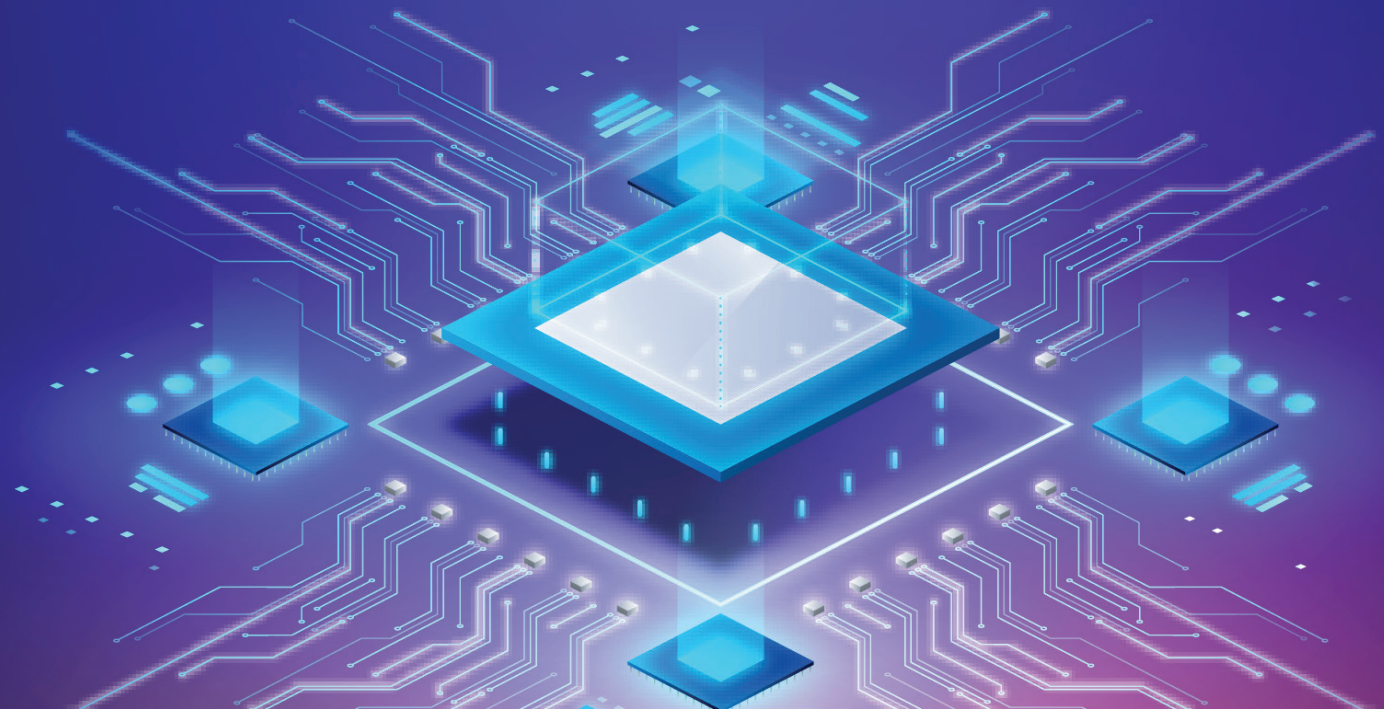
THE SILICON ROADMAP

Insights from

Semiconductor Ecosystem Conference
SEC 2025



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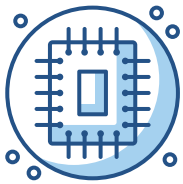


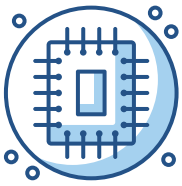
Executive Summary

India's Semiconductor Blueprint: From Vision to Visible Progress

The Maharashtra Chamber of Commerce, Industries and Agriculture (MCCIA) successfully conducted its second Semiconductor Ecosystem Conference in Pune on October 10, 2025, marking a significant milestone in India's transition from semiconductor aspiration to tangible execution. The conference brought together distinguished industry leaders, policymakers, international partners, and academic institutions to examine India's evolving semiconductor landscape and chart concrete pathways toward technological self-reliance.

Mr. Prashant Girbane, Director General of MCCIA, opened the conference by emphasising the organisation's nine-decade legacy as a bridge between industry, government, and academia. He highlighted MCCIA's commitment to capability enhancement, noting that over 13,000 enterprises across Maharashtra benefitted from 200+ training programmes in the past year, including an applied AI workshop across 12 districts. Girbane stressed that building a semiconductor ecosystem requires collective ownership and urged participants to treat the conference as an opportunity for meaningful collaboration rather than passive listening.

Mr. Sanjeev Keskar, Convenor of SEC 2025, provided compelling context drawn from his thirty-five years in the semiconductor industry. He noted that India's semiconductor market, currently valued at USD 30 billion, and is projected to reach USD 100 billion by 2030, expanding the country's global share from six to ten percent. This growth sits within a broader electronics industry trajectory toward USD 400 billion, driven by smart phones, automotive applications, data centres, AI adoption, and 5G infrastructure. Keskar emphasised the urgent need to move up the value chain from electronics manufacturing toward semiconductor design and component manufacturing, noting that roughly half the value in electronics lies in components whilst one-quarter resides in semiconductors.



Mr. Sushil Pal, Joint Secretary at MeitY and a key architect of India's Semiconductor Mission, delivered the keynote address highlighting that electronics production has grown at nearly 30% annually. He shared that under ISM 1.0; the Government of India has approved ten diverse projects covering silicon CMOS fabs, compound fabs, and advanced ATMP units, with USD 10 billion in national incentives. The Electronic Component Manufacturing Scheme received overwhelming response with 249 proposals worth over ₹1.1 lakh crore.

Pal explained that India's immediate opportunity lies in 28nm and above nodes where both domestic demand and technological partnerships are mature, whilst acknowledging that sub-5 nanometre fabrication demands investments and market readiness still developing.

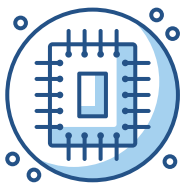
Throughout various panel discussions, industry leaders identified persistent ecosystem challenges and opportunities. Mr. Ashok Mishra of Arethra Technologies warned that "our start-ups are learning to take off, but many don't have enough fuel to land," highlighting insufficient capital flow and the "Gora Syndrome" where Indian OEMs prefer imported technologies over domestic innovations. Mr. K. Sridhar from SFAL advocated for regional specialisation with Pune focusing on automotive and embedded electronics, whilst Mr. Kausik Mandal from L&T Semiconductor Technologies stressed the importance of developing a product mindset beyond India's traditional service excellence.

The manufacturing panel, moderated by Mr. Sudeep Gupta of Alphawave, showcased tangible progress. Mr. Raghu Panicker from Kaynes SemiCon emphatically corrected perceptions: "We should stop saying factories are 'setting up'—they're already set up. Pilot production is happening." Ms. Apoorva Raut from RRP Electronics detailed her company's journey achieving pilot production within six months, whilst Mr. Bing Xue from Alpha & Omega Semiconductor confirmed that exponential India market growth and customer diversification requirements drove their partnership decisions.

International collaboration emerged as essential through the global partnerships panel featuring perspectives from Israel, Germany, Taiwan, the United States, and Sweden. Ms. Kristy Hsu from CIER Taiwan advocated for India focusing on mature technologies before advancing to cutting-edge nodes, whilst Mr. Aditya Fuke from Fraunhofer-Gesellschaft highlighted Germany's technological depth in compound semiconductors.

The skilling panel addressed talent development challenges. Mr. S.D. Sudarsan from CDAC outlined the transformative Chip to Start-up programme scaling from 350 students five years ago to targeting 100 tape-outs annually with a "One Tape One Student" initiative. Prof. Maryam Shojaei Baghini from IIT Bombay emphasised developing "semiconductor thinkers, not just designers," noting that innovation requires fundamental thinking rather than rote tool usage.

The summit concluded with consensus that India's semiconductor revolution is actively unfolding with operational facilities, robust policy frameworks, and scaling talent initiatives. As Maharashtra's second dedicated semiconductor ecosystem conference, this event positioned MCCIA as a catalyst for collaborative innovation, demonstrating that semiconductor self-reliance represents both strategic necessity and achievable reality when industry, academia, and government move in unison toward shared technological leadership goals.



Welcome Address

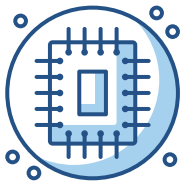
MCCIA's Role in Building India's Semiconductor Future

Prashant Girbane
Director General, Mahratta Chamber of Commerce, Industries and Agriculture (MCCIA)

Mr. Prashant Girbane, Director General of the Maharashtra Chamber of Commerce, Industries and Agriculture (MCCIA), set the tone for the day by expressing his enthusiasm for the conversations to follow, remarking that such gatherings hold immense value in shaping Pune's—and India's—technological future. Reflecting on MCCIA's nine-decade legacy, Mr. Girbane briefly traced its journey since its establishment in 1934. Over the years, the Chamber has evolved into one of the most respected industry associations in the country. Representing the collective voice of its board, committee chairs, and members, he noted that MCCIA continues to be a bridge between industry, government, and academia. Outlining the organisation's key functions, he highlighted MCCIA's advocacy efforts, capacity-building initiatives, and ecosystem development programmes. Each year, the Chamber engages with nearly 20 ministers and over 30 secretaries at the state and central levels, raising issues that matter to industry. He then spoke about MCCIA's strong commitment to capability enhancement, particularly for MSMEs. In the past financial year alone, more than 13,000 enterprises across Maharashtra benefitted from over 200 training programmes designed to improve competitiveness, digital readiness, and management practices. One notable initiative, an applied AI workshop conducted across 12 districts, helped a thousand MSMEs adopt simple artificial intelligence tools to improve efficiency.

Mr. Girbane also emphasised MCCIA's work in building long-term industrial infrastructure, including its role in developing clusters that drive sustained collaboration. The Auto Cluster, he noted, has served over 750 MSMEs last year alone, offering shared testing and validation facilities that strengthen Pune's manufacturing ecosystem. Closer to the theme of the day, he spotlighted the MCCIA Electronic Cluster Foundation (MECF), established with support from the Ministry of Electronics and IT (MeitY), the Government of Maharashtra, and MCCIA itself, which provides advanced testing, EMI/EMC validation, and prototype design facilities to hundreds of electronics manufacturers. He

acknowledged the collective efforts of industry leaders, institutional partners, and individuals who make such initiatives possible, thanking the chairs of various sectoral committees for their active involvement. Turning to the conference theme, Mr. Girbane urged participants to treat such events not merely as forums for listening but as opportunities for meaningful interaction and collaboration. With a touch of humour, he compared conferences to family weddings—where, beyond the ceremony itself, the true value often lies in the connections made. “The purpose is not just to attend, but to meet, exchange, and find people you can build with,” he remarked. Concluding his address, he encouraged the audience to work towards a shared language and direction for India’s semiconductor ecosystem. While experts would define the technical architecture, he said, it is equally essential for individuals, institutions, and enterprises to move in unison. “At the end of the day,” he observed, “building an ecosystem—just like building a city—requires smooth roads, accessible systems, and collective ownership.” With that thought, he set the stage for the day’s deliberations, inviting everyone to participate wholeheartedly in shaping the roadmap for India’s silicon future.



Opening Remarks

Charting India's Path in the Global Semiconductor Value Chain

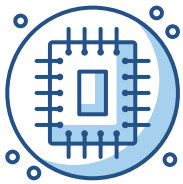
Sanjeev Keskar
Convenor, SEC2025

Mr. Sanjeev Keskar, Convenor of SEC 2025, opened the conference by setting a compelling context for the day's deliberations. Drawing upon his thirty-five years of experience in the semiconductor industry and his more recent work as a consultant supporting start-ups in the electronics domain, he reflected on the remarkable transformation unfolding in India's semiconductor landscape. He observed that India stands at a defining moment, poised to play a far greater role in the global value chain, and that the discussions throughout the day would seek to translate this potential into actionable outcomes for Maharashtra and for the nation at large. He began by mapping the global trajectory of the semiconductor sector, which currently stands at an estimated value of USD 600 billion and is projected to surpass the USD 1 trillion mark by 2030. Given that semiconductors traditionally account for around one-quarter of the global electronics market, the broader electronics industry is expected to reach nearly USD 4 trillion within the same period. Against this backdrop, India occupies a uniquely advantageous position: almost one-fifth of the world's semiconductor design workforce is based in the country, signalling both its technical capability and its strategic relevance to the global ecosystem. The domestic market, valued at approximately USD 30 billion today, is projected to grow to USD 100 billion by 2030, expanding India's share of the global semiconductor space from six to ten per cent. This growth, Mr. Keskar noted, would be driven by an array of sectors—from smart phones, consumer and industrial electronics, and automotive applications to data centres, AI adoption, and the rapid development of 5G and IoT infrastructure. Collectively, these drivers are expected to push India's electronics industry to nearly USD 400 billion by the end of the decade.

Elaborating on the semiconductor value chain, he explained that it begins with electronic design automation tools and chip design, progresses through wafer fabrication and assembly-testing-packaging stages, and culminates in product manufacturing. At present, India's contribution is concentrated in

electronics manufacturing services, especially mobile-phone assembly, which generates only a fraction of total value addition. Mr. Keskar emphasised the urgent need to move up the chain towards semiconductor design, component manufacturing, and product innovation, pointing out that roughly half of the value in electronics lies in components, one-quarter in semiconductors, and the remaining share in design and innovation. He commended the significant policy impetus provided by the India Semiconductor Mission, which has approved ten proposals and encouraged several others already in development, supported by a USD 10 billion national incentive. He also welcomed the government's focus on the electronic component manufacturing ecosystem, which has received 249 proposals worth over ₹1.1 lakh crore under the recently launched scheme for passive and display components. Such developments, he said, mark a critical step towards building a self-reliant and comprehensive electronics ecosystem in the country.

Turning his attention to Maharashtra, Mr. Keskar noted that while several fabrications and ATMP units are emerging across other states, none of the sanctioned projects are currently located in Maharashtra. He called upon stakeholders to strengthen the state's positioning by developing a complete ecosystem encompassing compound semiconductors, display fabrication, EMS expansion, and capital-equipment manufacturing. He urged the state government to proactively engage with companies submitting proposals under national schemes and attract them through targeted incentives, thereby fostering synergies between design, manufacturing, and innovation within the region. He further underscored Pune's potential to emerge as a design hub, given its strong base of multinational semiconductor design centres such as NXP and Alpha, and welcomed the forthcoming STPI incubation and testing facility that promises to nurture fabless and embedded-system start-ups. Mr. Keskar concluded his address by commending the organising team for their meticulous preparation and expressing confidence that the day's discussions would yield valuable insights for strengthening India's semiconductor and electronics ecosystem. "The semiconductor revolution," he remarked, "is already in motion, and Maharashtra must seize this moment to position itself at its very core."



Special Address 1

STPI's Commitment to Nurturing India's Fabless and Design Ecosystem

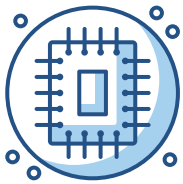
Mr. Ajay Prasad Shrivastava
Director, STPI Pune

Mr. Ajay Prasad Shrivastava, Director of the Software Technology Parks of India (STPI) Pune, delivered the first Special Address of the conference, weaving together a personal narrative and a vision for collaborative growth in Maharashtra's semiconductor ecosystem. Speaking with candour and warmth, he reflected on his journey within STPI, an organisation with which he has been associated for over twenty-six years, and shared his conviction that the success of India's semiconductor mission will rest on collective effort, integrity, and the passion to innovate. He began by recalling his early years with STPI in Rajasthan and his seventeen-year tenure in Chandigarh, where he had the opportunity to establish one of the largest incubation centres in the country, dedicated to artificial intelligence and data analytics. This centre, which included a 200-terabyte standard data facility, stood adjacent to the Semiconductor Laboratory—an experience that allowed him to work closely with semiconductor professionals and develop a deep understanding of the sector's complexities. He described this phase as the foundation that shaped his later vision of nurturing semiconductor design talent and fostering home-grown innovation.

When he was transferred to Pune, he said, he arrived in an unfamiliar city with little personal connection but a strong determination to make an impact. He narrated how his association with MCCIA began serendipitously—staying near the Chamber's office, being introduced to its network through colleagues from IIT Bombay, and soon finding himself connected with the organisation's leadership. Within weeks, he witnessed what he called "the power of MCCIA"—a community that not only facilitates business linkages but also builds trust, governance, and meaningful partnerships. Quoting a senior government official who had visited Maharashtra for industry consultations, Mr. Shrivastava highlighted that MCCIA's strength lies not merely in initiating projects but in the excellence of its governance and the sincerity with which it executes them. He expressed deep appreciation for MCCIA's proactive role in promoting MSMEs and the electronics sector across Maharashtra, and shared

his excitement about the collaboration between STPI and the Chamber to establish a Centre of Excellence in Semiconductor Design. Unlike other emerging technologies such as AI, blockchain, or IoT—where STPI already runs twenty-four centres of excellence nationwide—he emphasised that semiconductor development presents a far greater entry barrier, requiring substantial resources, sustained coordination, and multi-stakeholder commitment. In this regard, he acknowledged the efforts of industry leaders and partners such as Shri Shridhara and expressed optimism that their collective experience would help accelerate Pune's progress in this domain.

Mr. Shrivastava underscored that STPI's role extends beyond infrastructure; its essence lies in fostering innovation and mentorship. With a network of sixty-eight centres across India, STPI Pune, he said, is well positioned to become a key node in India's semiconductor design ecosystem. The upcoming 600-seat incubation facility at Hinjawadi is envisioned as a hub for fabless start-ups, providing the necessary technical and business support to nurture indigenous IP creation and product design. He described Pune as uniquely suited for this endeavour—a city that combines the industrial dynamism of "the Detroit of India" with the intellectual depth of "the Oxford of the East." Its abundance of technical talent and its culture of ethical professionalism, he said, make it the ideal location for India's next wave of semiconductor innovation. Concluding on an inspiring note, he urged all stakeholders—academia, industry, and government—to work together with integrity and shared purpose. "Passion drives a start-up," he remarked, "but only collaboration sustains it. If we remain ethical and united, the next generation of semiconductor designs stamped 'Made in Pune' will become a reality."



Special Address 2

India's Semiconductor Breakthrough: Leadership, Capability and Momentum

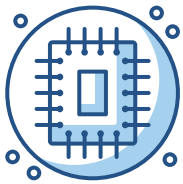
Mr. Vinayak Pai
MD & CEO, TATA Projects

Mr. Vinayak Pai, Managing Director and CEO of Tata Projects, delivered a powerful and forward-looking address on India's emerging leadership in the semiconductor sector. Speaking with conviction and clarity, he emphasised that what once seemed like a distant ambition has now materialised into an extraordinary national achievement, with India successfully producing its first indigenous semiconductor chip, an outcome that reflects the country's determination, capability, and unity of purpose. He began by acknowledging the strong participation of industry leaders, policymakers, and entrepreneurs in the event, describing it as a reflection of the growing interest and enthusiasm surrounding India's semiconductor journey. Only a few years ago, he recalled, India was taking its initial steps in electronics manufacturing—assembling mobile phones and producing outer casings for global brands such as Apple. At that time, the idea that a semiconductor chip could be designed and fabricated in India by 2025 would have seemed improbable. Yet, that vision has already been realised, with the first "Made in India" chip being launched earlier this year in Noida. This, he noted, symbolises the beginning of a new technological era for the nation.

Mr. Pai attributed this rapid transformation to two critical forces—the unwavering commitment of the Government of India and the intellectual strength of the Indian talent pool. He highlighted the strategic clarity and policy leadership demonstrated through the India Semiconductor Mission (ISM), under the stewardship of leaders such as Prime Minister Narendra Modi, Minister Ashwini Vaishnaw, and the team at MeitY. The first iteration of ISM, followed now by ISM 2.0, has created a globally competitive environment for semiconductor manufacturing. International observers, he remarked, have noted with surprise that India's policy incentives are even more attractive than those offered under the United States' CHIPS Act—an unprecedented shift that has positioned India as a serious global contender in this domain.

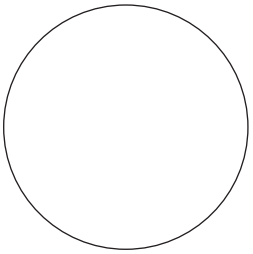
Equally important, he said, is the intellectual contribution of Indians across the global semiconductor value chain. From Micron's leadership in the United States to returnees such as Dr. Randhir Thakur—now leading Tata Electronics—Indian professionals have played a decisive role in shaping the global industry. Recounting his own experience working with Micron's project in Gujarat, Mr. Pai shared how nearly every senior figure he encountered, from Sanjay Mehrotra to Manish Bhatia, had Indian roots. This convergence of global expertise and domestic opportunity, he said, has been instrumental in India's swift progress. Drawing from Tata Projects' direct involvement in several of the first semiconductor initiatives under ISM, Mr. Pai spoke about the immense technological complexity and precision required to build fabrication and OSAT facilities. Comparing it with his prior experience in the oil and gas sector, he described semiconductor fabs as "engineering marvels of another order"—vast, million-square-foot ecosystems with half a million square feet of clean room infrastructure, housing some of the most advanced process technologies in the world. He praised the government's ambition to achieve global benchmarks in record time, challenging project developers to deliver in 18 months or less—demonstrating both urgency and belief in India's capability to execute.

He emphasised that the future success of India's semiconductor industry will depend on three foundational pillars: technological development, supply chain resilience, and skill creation. The first, he said, requires academia, research institutions, and industry to co-create indigenous technologies, strengthening domestic design and manufacturing capabilities. The second, an integrated supply chain, must evolve beyond dependence on foreign suppliers, drawing lessons from India's achievements in the pharmaceutical and clean manufacturing sectors to build a robust local ecosystem. He envisioned this as a space where MSMEs could play a pivotal role, providing specialised tools, materials, and logistics support around every semiconductor facility. The third and perhaps most vital element, he stressed, is talent. India must focus on developing a skilled workforce across design, operations, and maintenance—an area where cities like Pune, with their strong educational and industrial base, can become national centres of excellence. Concluding his address, Mr. Pai reiterated that the semiconductor revolution is no longer a distant dream but a living reality taking shape before our eyes. The pace of transformation witnessed under ISM 1.0 and 2.0, he said, demonstrates that India can achieve in two years what others take a decade to accomplish. He urged industry, academia, and government stakeholders to continue working together with the same momentum, collaboration, and clarity of purpose that have brought the nation this far. "If we get technology, supply chain, and skills right," he remarked, "India will not just participate in the global semiconductor industry—it will lead it."



Keynote Address

Policy, Scale and Strategy: MeitY's Roadmap for Semiconductor Growth



Mr. Sushil Pal
Joint Secretary, MEITY

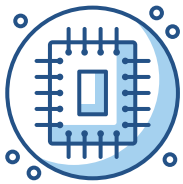
Delivering the keynote address, Mr. Sushil Pal, Joint Secretary at MeitY, offered a comprehensive overview of India's evolving semiconductor and electronics landscape, while highlighting the strategic direction and policy framework driving its transformation. Widely regarded as one of the key architects of India's Semiconductor Mission, Mr. Pal's address underscored the government's commitment to building a robust domestic manufacturing and design ecosystem rooted in innovation, collaboration, and sustainability. He began by extending his appreciation to MCCIA for organising the Semiconductor Ecosystem Conference, which he described as an "important platform bringing together industry, academia, and start-ups under one roof." Apologising for his inability to attend in person, he emphasised how such forums play a vital role in shaping dialogue, aligning stakeholder efforts, and accelerating India's vision of becoming a trusted global hub for semiconductor and high-tech manufacturing.

Tracing India's electronics journey, Mr. Pal noted that while the country was a late entrant to large-scale electronics manufacturing, the past decade has seen remarkable progress. Electronics production in India, he said, has grown at an annual rate of nearly 30%, and exports have been rising steadily as well. Although India's manufacturing base remains modest compared to leading economies, its trajectory is clear—targeting 25% of GDP from manufacturing, with electronics and semiconductors forming the bedrock of that ambition. "Electronics has become a foundational industry," he remarked, "one that supports and enables every other sector of manufacturing." Mr. Pal elaborated on the multi-layered policy ecosystem that underpins this growth—the Production Linked Incentive (PLI) schemes for large-scale electronics, IT hardware, and electronic components; the DLI (Design Linked Incentive) scheme; and the flagship India Semiconductor Mission (ISM).

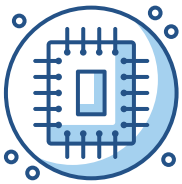
Collectively, these initiatives aim not only to attract global investments but also to strengthen domestic capabilities across the semiconductor value chain.

He shared that under ISM 1.0, the Government of India has approved ten diverse projects covering the full spectrum of semiconductor manufacturing—from silicon CMOS and compound fabs to advanced ATMP (Assembly, Testing, Marking, and Packaging) units. Each of these, he explained, is strategically designed to serve specific market segments such as power electronics, display ICs, and RF devices. For instance, one of the approved ATMP facilities will focus on high-density 3D packaging, integrating chips and passive components on a single substrate—an innovation that would position India among the global pioneers in advanced semiconductor packaging technologies. Addressing the often-raised question of why India has not yet moved towards sub-5 nanometre fabrication, Mr. Pal explained that such facilities demand massive investments and market readiness that are still developing. "At present, India's immediate opportunity lies in 28 nm and above nodes, where both domestic demand and technological partnerships are already mature," he said. He highlighted the government's approach of leveraging technology collaborations with established international players to fast-track execution while minimising redundant R&D expenditure.

Mr. Pal also reaffirmed MeitY's commitment to ensuring timely and efficient project implementation, acknowledging Tata Projects' role in spearheading complex fab construction efforts with world-class precision. Beyond manufacturing, he stressed the importance of nurturing indigenous design capabilities. While India already accounts for roughly 30% of the world's chip design talent, much of it serves multinational corporations. He encouraged industry bodies like MCCIA to support local design start-ups in developing and marketing their own products, ensuring that design innovation translates into commercial and intellectual value retained within the country. Expanding his address beyond semiconductors, Mr. Pal provided updates on the broader electronics ecosystem. The PLI for large-scale electronics manufacturing, he said, has been India's most successful industrial incentive scheme, leading to record exports of smart phones and attracting global majors such as Apple and Google to establish local production. The IT hardware PLI, though initially slow, is now witnessing renewed interest and substantial investment, while the Electronic Component Manufacturing Scheme (ECMS) has received overwhelming response from industry stakeholders. He explained that ECMS was designed after deep consultation with manufacturers to offset specific cost disabilities—whether in multilayer PCBs, high-density interconnects, or capacitor manufacturing—through a flexible mix of PLI and capital subsidies.



Turning his focus to Pune, Mr. Pal lauded the city's unique position in India's technological and industrial ecosystem. As a leading hub for automotive manufacturing, he said, Pune stands at the cusp of a new revolution where vehicles are increasingly becoming "computers on wheels." The transition to electric and autonomous mobility will significantly raise the demand for semiconductor content, and Pune's strong base of MSMEs, engineering talent, and R&D institutions positions it ideally to lead this transformation. He also urged MCCIA to focus on emerging domains such as circular economy and industrial automation—both critical for sustainable manufacturing and global competitiveness. Concluding his keynote, Mr. Pal expressed confidence that India's semiconductor and electronics ecosystem is on an irreversible path of growth. "Our policies have evolved from vision to action," he said. "Now it is time for execution—with industry, academia, and government moving in unison. Together, we can make India not only a participant but a leader in the global semiconductor value chain."



Inaugural Address

Building Momentum: Maharashtra's Collective Push for a Semiconductor Ecosystem

Mr. Ajit Chigteri
Group Lead, SEDG

Delivering the vote of thanks, Mr. Ajit Chigteri extended heartfelt appreciation on behalf of MCCIA to all participants who contributed to the success of the conference. Marking the second edition of this initiative—following the inaugural event held on July 15, 2024—he announced plans to continue this momentum with another session scheduled in six months, reaffirming MCCIA's commitment to nurturing Maharashtra's semiconductor ecosystem.

Mr. Chigteri expressed gratitude to the distinguished dignitaries whose presence and insights elevated the conference. He acknowledged Mr. Sushil Pal for joining remotely despite his busy schedule, Mr. Vinayak Pai for his participation amid pressing commitments, Mr. Ajay Prasad from STPI, Mr. Sanjeev Keskar who travelled from Bangalore to serve as a guiding force, and Mr. Prashant Girbane along with the entire MCCIA team. He noted that their words of wisdom had set a high benchmark for the day's deliberations.

Special recognition was extended to sponsors and partners whose support proved vital: Software Technology Parks of India, with particular mention of Mr. Vivek Anand for his exceptional coordination; Killer Ground Engineering Private Limited; MCCIA Electronic Cluster Foundation; and Mrs. Rikushna Gartil. Mr. Chigteri appreciated participants for attending on a Friday, acknowledging the personal commitment required to join despite weekend plans.

He concluded by emphasising that the conference serves as an important platform for fostering dialogue and collaboration toward building a robust semiconductor ecosystem in Pune and across Maharashtra—an integral component of the Atmanirbhar Bharat mission championed by Prime Minister Narendra Modi. "Together," he said, "we can pave the way for innovation and self-reliance in this critical sector."

Panel Discussion 1

Beyond Manufacturing: Building India's Semiconductor Competence Chain

Panelists:

Mr. Sudeep Gupta
ND India, Alphawave (Moderator)

Mr. Ashok Mishra
Semiconductor Technology Advisor

Mr. Ashwani Bhat
VP Engineering, Lattice Semiconductor

Mr. K. Sridhar
CEO, Sfal

Mr. Kausik Mandal
L&T Semiconductor Technologies

The panel on "Beyond Fabs: Driving Semiconductor Self-Reliance" brought together industry veterans who explored India's evolving semiconductor ecosystem, discussing challenges, opportunities, and actionable solutions for building long-term self-reliance. The session was moderated by Mr. Sudeep Gupta, Managing Director – India, Alphawave, and Executive Committee Member, IESA. The panellists included Mr. Ashok Mishra, Semiconductor Technology Advisor and Founder, Arethra Technologies; Mr. Ashwani Bhat, Vice President – Engineering, Lattice Semiconductor; Mr. K. Sridhar, CEO, SFAL (Semiconductor Fabless Accelerator Lab); and Mr. Kausik Mandal, L&T Semiconductor Technologies.

Mr. Sudeep Gupta
ND India, Alphawave
(Moderator)

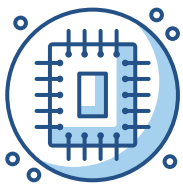
"I believe that semiconductor self-reliance doesn't mean isolation — it means having control over critical systems that define national strength."

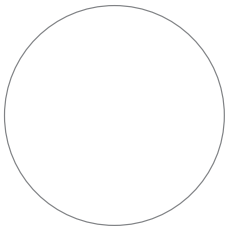
Opening the discussion, Mr. Gupta framed semiconductor self-reliance not as an aspiration for total independence but as the pursuit of control over the most critical technologies in the value chain — from design and packaging to validation and system integration. He observed that no nation, not even the United States or China, is entirely self-sufficient in semiconductors, yet each has strategically developed areas of control vital to their security and competitiveness. He set the agenda for the discussion to move beyond rhetoric and identify practical actions that organisations like MCCIA could take within a year to strengthen India's position. Mr. Gupta emphasised that the focus must lie on ecosystem readiness, nurturing domestic design capability, and building the infrastructure required for post-silicon testing and validation — essential steps for translating India's intellectual strength into manufacturing capability.

Mr. Ashok Mishra
Semiconductor Technology
Advisor

"Our start-ups are learning to take off, but many of them don't have enough fuel to land."

Speaking from the standpoint of a founder deeply embedded in the semiconductor start-up ecosystem, Mr. Mishra dissected the three vital enablers of a thriving innovation landscape — access to capital, talent, and markets. While the global hype around semiconductors has brought some investor attention, the capital flow remains limited and insufficient for long-cycle, capital-intensive ventures. He likened the predicament to aircraft running out of fuel mid-air — start-ups that begin promisingly but lack funds to sustain their journey. He also raised the issue of domestic market access, arguing that Indian OEMs seldom source from Indian innovators, preferring imported technologies instead — a mindset he termed the "Gora Syndrome." Mr. Mishra urged industry stakeholders to prioritise Swadeshi investments, creating space for Indian fabless companies to grow. He warned that unless India consciously nurtures indigenous IP and product companies, it risks repeating the fate of its once-promising mobile manufacturing industry, which failed to build technological depth despite early market dominance.

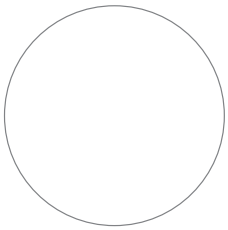




Mr. Ashwani Bhat
VP Engineering, Lattice Semiconductor

"Our challenge is not just about talent — it's about building the ecosystem that allows that talent to perform."

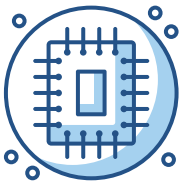
Bringing a multinational perspective, Mr. Bhat spoke about Lattice Semiconductor's journey in India and its recent expansion into Pune. He highlighted the logistical and regulatory hurdles that companies face, from import clearances to establishing specialised facilities. Despite these obstacles, he expressed optimism about Pune's potential, revealing that Lattice's Pune centre houses diverse teams working on FPGA design, AI and ML architecture, and EDA tools. He emphasised the significance of post-silicon validation, which ensures that designed chips are production-ready — an area India must rapidly develop. Mr. Bhat proposed that public policy support and industry collaboration could catalyse the establishment of such facilities, turning Pune into a hub for design validation and advanced electronics testing. He also stressed the importance of developing specialised talent pools, suggesting stronger partnerships between academia and industry to ensure that engineers are not just trained but also "industry-ready."

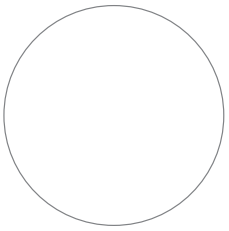


Mr. K. Sridhar
CEO, Sfal

"Every state needs its own SFAL — because one national team cannot win every match."

Reflecting on SFAL's model in Karnataka, Mr. Sridhar explained how the organisation's industry-led, government-supported structure has proven instrumental in nurturing semiconductor start-ups. SFAL's success, he said, comes from its collaborative approach — bringing together mentors from established MNCs, venture capital networks, and government agencies to offer holistic support to entrepreneurs. He emphasised the need for regional specialisation, suggesting that every state develop focus areas aligned with its existing industrial strengths — Pune and Maharashtra, for instance, could emerge as a centre for automotive and embedded electronics, while Karnataka continues to focus on high-performance computing. He noted that market orientation, not just technology creation, must drive innovation. By helping start-ups refine product positioning, connect with VCs, and access global markets, initiatives like SFAL bridge the critical gap between design and deployment. Mr. Sridhar concluded that India's semiconductor dream cannot rest on a single institution — it requires a network of state-level innovation clusters working in sync.





Mr. Kausik Mandal
L&T Semiconductor Technologies

"India has brilliant engineers — but we need to transform them from service experts into product creators."

Representing L&T Semiconductor Technologies, Mr. Mandal discussed the persistent structural bottlenecks that prevent India from realising its full potential — notably, limited access to foundries, ESD libraries, and testing infrastructure. Despite funding, Indian companies still depend heavily on overseas facilities for chip fabrication and validation. He stressed that self-reliance would materialise only when the entire chain — from design and packaging to production — is available within India. Mr. Mandal further emphasised the importance of developing a product mindset, observing that while India excels in services, it still lacks depth in product ownership and lifecycle thinking. He proposed that academic curricula integrate product management as a core discipline — a skill that bridges technology creation and commercialisation. Advocating for practical collaboration, he recommended the formation of micro-consortia — small, outcome-oriented partnerships between academia, start-ups, and industry — focused on measurable goals in packaging, testing, and skill development. "Run consortia for results, not rituals," he remarked.

Presentation by Accurate

Precision Engineering for India's Semiconductor Manufacturing

Mr. Gopal Vaidyanathan

CEO of Accurate's Onyx Robotic and Automation Division

Mr. Gopal Vaidyanathan, CEO of Accurate's Onyx Robotic and Automation Division, outlined his company's strategic positioning to support India's emerging semiconductor ecosystem, leveraging six decades of precision engineering expertise.

Founded in 1963, Accurate has evolved from manufacturing basic measuring instruments to becoming India's largest market shareholder for Coordinate Measuring Machines (CMMs). The ISO 9001:2015 certified company exports to 27 countries and maintains an extensive network of service offices and calibration laboratories nationwide. Its CMM portfolio ranges from tabletop units to systems large enough to accommodate entire metro carriages, serving major clients including Bosch, Indian Railways, and virtually every automobile manufacturer in India.

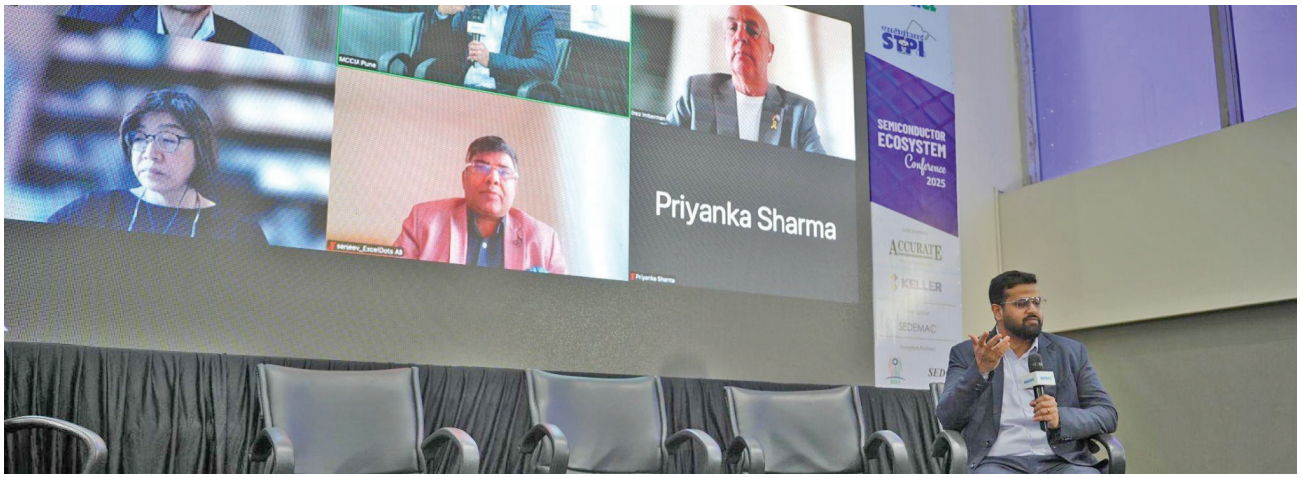
Mr. Vaidyanathan explained that the Onyx Division, established in 2023, focuses on advanced automation for the 3C sector, particularly Final Assembly, Test, and Pack (FATP) lines for smart phone manufacturers in southern India. The division currently maintains over 2,500 machines across multiple sites, demonstrating operational excellence in high-volume, precision-critical environments.

Building on this foundation, Accurate is now preparing to serve the semiconductor industry through three key offerings: precision tooling components for fabrication equipment, comprehensive on-site support services (OSS) including new product introduction, troubleshooting, calibration and audits, and equipment lifecycle management from line bring-up through long-term sustenance.

Addressing India's skills gap, Mr. Vaidyanathan announced the establishment of Accurate Academy at the company's Chakan facility, with expansion planned for Jejuri. The training institute prepares fresh graduates for precision manufacturing roles and is ready to develop semiconductor-specific curricula in partnership with MCCIA and industry stakeholders.

He concluded by inviting collaboration to localise semiconductor equipment support capabilities, positioning Pune as a vital contributor to India's semiconductor self-reliance ambitions.

Panel Discussion 2



Collaborating for Resilience: International Perspectives on Semiconductor Growth

Panelists:

Mr. Erez Imberman
Ex-VP, Tower Semiconductor, Israel

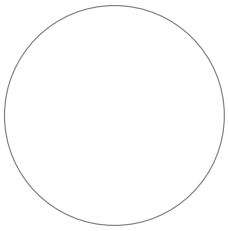
Mr. Aditya Fuke
Sr. Manager, Fraunhofer-Gesellschaft, Germany

Ms. Kristy Hsu
Director, CIER, Taiwan

Dr. Sanjay Bhandari
CEO, Vibrant Microsystems, USA

Mr. Sanjeev Sharma
CEO, ExcelDots AB, Sweden

The panel convened international experts to explore strategic partnerships and collaborative opportunities that could accelerate India's semiconductor ambitions. The session brought together representatives from Israel, Germany, Taiwan, the United States, and Sweden, each offering unique perspectives on technology transfer, market access, and ecosystem development. The panellists included Mr. Ere Imberman, Ex-VP, Tower Semiconductor, Israel; Mr. Aditya Fuke, Sr. Manager, Fraunhofer-Gesellschaft, Germany; Ms. Kristy Hsu, Director, CIER, Taiwan; Dr. Sanjay Bhandari, CEO, Vibrant Microsystems, USA; and Mr. Sanjeev Sharma, CEO, ExcelDots AB, Sweden.



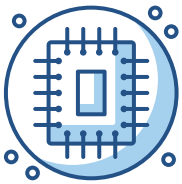
Mr. Erez Imberman
Ex-VP, Tower Semiconductor, Israel

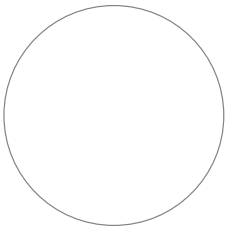
"India must consider very seriously the time it takes to develop semiconductor capabilities — forums like these are a good start."

Opening the discussion from Israel's perspective, Mr. Imberman brought extensive experience from Tower Semiconductor and his current engagement with Israeli government initiatives supporting global semiconductor partnerships. He acknowledged that India's semiconductor journey, initiated under the India Semiconductor Mission by Prime Minister Modi and supported by Ministers Ashwini Vaishnaw and the broader team, represents a significant policy shift. While he noted the progress made over the past decade with approximately 10-15 projects already underway, he candidly acknowledged the sector's challenges, particularly the extended timelines required to build manufacturing capacity.

Mr. Imberman emphasized that India's global collaborations span multiple geographies including the US, Europe, Japan, Korea, Taiwan, and Singapore, focusing on attracting OEMs, establishing supply chains, and building the currently non-existent semiconductor ecosystem. He recognized the fundamental difficulties India faces: supply chain dependency, infrastructure gaps, and the inherent complexity of semiconductor manufacturing. However, he positioned Israel as a valuable partner for India, suggesting that Israeli companies could collaborate with Indian enterprises to provide market access and accelerate technology development.

His core message centred upon patience and realistic expectations. Drawing from Israel's own experience, he stressed that semiconductor capability development cannot be rushed, and that industry forums and collaborative platforms, though seemingly slow, represent essential starting points for building the relationships and knowledge transfer mechanisms needed for long-term success. He advocated for India to focus on creating the right enabling environment while acknowledging that reaching manufacturing maturity would require sustained effort over many years.





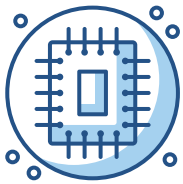
Mr. Aditya Fuke
Sr. Manager, Fraunhofer-Gesellschaft, Germany

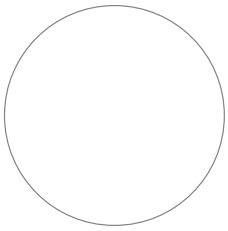
"India and Germany have a great opportunity to combine German technology expertise with India's growing potential and scale."

Speaking on behalf of Germany's premier applied research organization, Mr. Fuke presented Fraunhofer's extensive capabilities and its potential role in India's semiconductor ecosystem development. He outlined Fraunhofer's impressive scale: 75 research institutes with a budget of 8.6 billion Euros, 70% of which comes directly from industry partnerships. This model, where research is driven by commercial needs rather than purely academic pursuits, positions Fraunhofer as a bridge between laboratory innovation and market-ready technology.

Mr. Fuke highlighted Fraunhofer's semiconductor-specific strengths, including 30 institutes dedicated to electronics and microelectronics research, operating laboratories that maintain a 2-3 year technological lead over industry standards. The organization conducts 10,000 projects annually, with core focus on taking research from laboratory prototypes to near-commercialization stages. He detailed their comprehensive service portfolio: design services, multi-project wafer access, characterization and reliability testing, and process licensing — essentially offering end-to-end support from concept to pilot production.

A significant announcement was Fraunhofer's release of a knowledge paper during the COMPASS conference in India, which identified nine key collaboration areas between India and Germany. These collaborations leverage German technological depth in compound semiconductors, advanced analytics, and system reliability testing, combined with India's engineering talent and market potential. Mr. Fuke emphasized that scaling up skilled workforce development represents one of the most crucial elements for successful India-Germany semiconductor partnership, positioning education and training as foundational to all other collaborative activities.





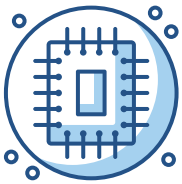
Ms. Kristy Hsu
Director, CIER, Taiwan

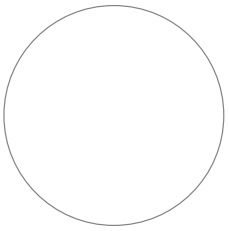
"India has the advantage of support from Western countries — this is very important for building a resilient supply chain."

Representing Taiwan's perspective, Ms. Hsu provided insights into the evolving Taiwan-India semiconductor relationship, contextualized within the broader geopolitical shift toward supply chain diversification. She explained that Taiwan has actively developed relations with India, particularly as global companies seek to reduce China dependency — a strategy often termed "China Plus One." Over the past five years, major Taiwanese electronics and ICT companies have increasingly viewed India as a critical alternative manufacturing destination, driven both by their own strategic considerations and by customer demands for diversified supply chains.

Ms. Hsu detailed several active collaborations, noting that Taiwanese companies have established operations in India ranging from OSAT (outsourced semiconductor assembly and test) facilities to design centres. She specifically mentioned that Taiwanese firms have been operating in India for nearly two decades in some cases, with one major company employing over 1,000 engineers in India for design and development work. However, she candidly acknowledged significant challenges in advanced packaging operations, indicating that while testing and design activities have successfully taken root, packaging capabilities still face considerable hurdles due to infrastructure and ecosystem gaps.

Drawing from a recent interview she gave to Indian Express, Ms. Hsu emphasized a pragmatic approach: India should focus on establishing capabilities in mature, proven technologies rather than attempting to immediately compete in cutting-edge nodes. She argued that building a solid foundation in established processes would create the ecosystem necessary for eventual advancement into more sophisticated technologies. Her message underscored the importance of patience and staged development, leveraging Taiwan's extensive experience in building semiconductor capabilities over decades rather than attempting accelerated leapfrogging that might compromise long-term sustainability.





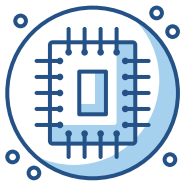
Dr. Sanjay Bhandari
CEO, Vibrant Microsystems, USA

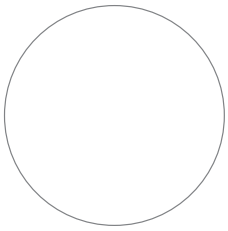
"The relationship between US and Indian companies is evolving — India is now creating its own path and all forms of collaboration are becoming possible."

Bringing a US perspective informed by extensive cross-border experience, Dr. Bhandari analyzed the transforming nature of US-India semiconductor collaboration. He noted that traditional partnerships historically focused on US product companies establishing design centres in India, leveraging Indian engineering talent for development work. However, the landscape has fundamentally shifted as India builds its domestic semiconductor ambitions, creating opportunities for more diverse and reciprocal partnerships.

Dr. Bhandari outlined the expanding collaboration possibilities: Indian fabs can now work with US companies, Indian fabless companies can leverage US resources and market access, and Indian OSAT facilities can serve global supply chains. He recognized India's successful track record in semiconductor services, citing companies in design, verification, and EDA tools that have established strong global reputations. Building on this foundation, he argued that India is well-positioned to expand into product development and manufacturing.

He identified several specific collaboration opportunities: licensing of technology and intellectual property from US firms, utilizing US-developed advanced packaging techniques, accessing sophisticated testing and validation infrastructure, and leveraging relationships with US-based equipment suppliers for advanced manufacturing tools. Dr. Bhandari emphasized that India should strategically utilize the management expertise, infrastructure knowledge, and supply chain relationships that US companies have developed over decades. His recommendation was for India to approach collaboration pragmatically, recognizing that while building indigenous capability is essential, strategic partnerships with established US players could significantly accelerate development timelines and reduce risks associated with technology adoption.





Mr. Sanjeev Sharma
CEO, ExcelDots AB, Sweden

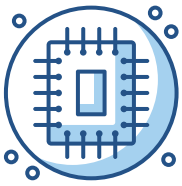
"If we have to be successful, we need to integrate advanced technologies — and for that we need to look at partnerships with Europe."

Concluding the panel from a European Union perspective, Mr. Sanjeev Sharma discussed how India could benefit from aligning its semiconductor policies with European initiatives, particularly the European Chips Act and associated programs. He began by contextualizing the semiconductor industry's trajectory, noting that it is expected to reach nearly one trillion dollars within five years, with growth concentrated in advanced applications such as AI, high-performance computing, and power electronics — areas where both India and Europe have strategic interests.

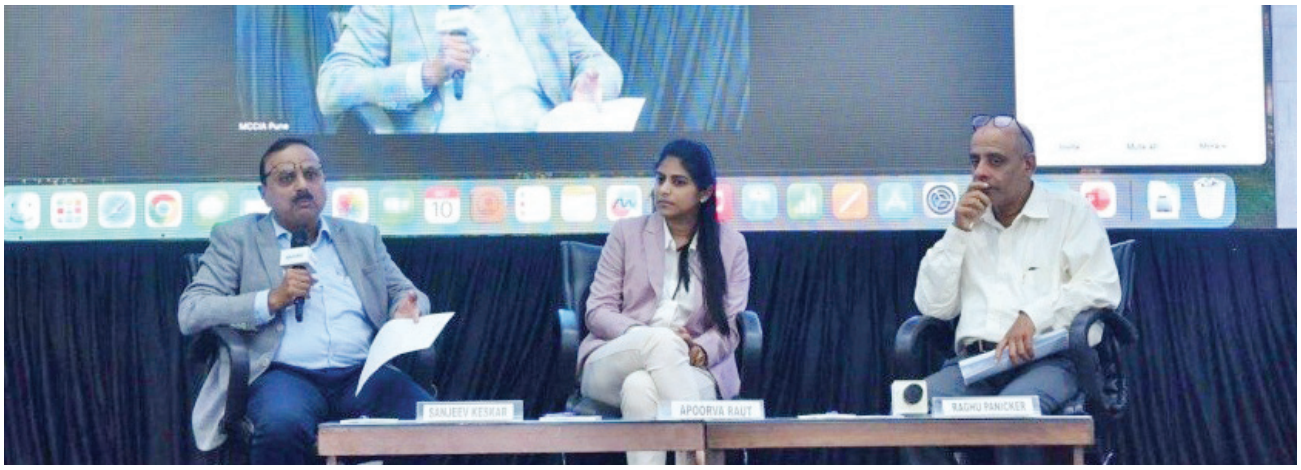
Mr. Sharma explained the European Chips Act's comprehensive approach, which includes over 40 billion Euros in commitments from public-private partnerships, and highlighted specific programs like Chips Joint Undertaking and the EU-India Trade and Technology Council. He emphasized that European initiatives focus heavily on advanced packaging technologies and specialized semiconductor applications, areas where collaboration with India could be mutually beneficial. He noted that India has strong research institutions actively engaged in semiconductor research, and partnerships with European counterparts could accelerate technology transfer and commercialization.

A significant portion of his presentation addressed workforce development, which he identified as one of Europe's largest challenges and a critical area for India-EU collaboration. The European Chips Act's first pillar focuses on competence development through workshops, cross-country exchange programs, and joint training initiatives sponsored by both governments and industry. Mr. Sharma argued that these programs could significantly benefit Indian engineers and researchers while also supporting European companies' supply chain diversification goals.

He concluded by emphasizing the importance of enabling investment corridors between India and Europe, facilitating not just technology transfer but also financial flows that would allow Indian companies to scale while supporting European supply chain resilience. His message was that realistic, practical collaboration requiring concrete investment mechanisms and institutional partnerships would yield more tangible results than aspirational declarations alone.



Panel Discussion 3



Inside India's OSAT Rise: Practical Realities and Industry Advances

Panelists:

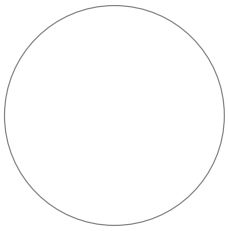
Mr. Sanjeev Keskar
CEO, Arvind Consultancy (Moderator)

Mr. Raghu Panicker
CEO, Kaynes SemiCon

Ms. Apoorva Raut
CTO, RRP Electronics

Mr. Bing Xue
EVP Global Sales, Alpha & Omega Semiconductor

The panel on "Strengthening the Semiconductor Manufacturing Ecosystem" brought together industry leaders actively establishing India's semiconductor manufacturing capabilities. The discussion focused on operational realities, practical challenges, and pathways to building a sustainable OSAT ecosystem in India. The session was moderated by Mr. Sanjeev Keskar, CEO, Arvind Consultancy, and featured Ms. Apoorva Raut, CTO, RRP Electronics; Mr. Bing Xue, EVP Global Sales, Alpha & Omega Semiconductor; and Mr. Raghu Panicker, CEO, Kaynes SemiCon.

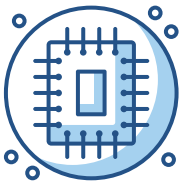


Mr. Sanjeev Keskar
CEO, Arvind Consultancy
(Moderator)

"India's electronics industry has been about local value addition — but at 15%, we're leaving $340 billion on the table by 2030."

Opening the session, Mr. Keskar framed India's semiconductor challenge through stark economics. With India's electronics market projected to reach $400 billion by 2030 but current value addition averaging only 15%, India would capture merely $60 billion of actual revenue while $340 billion flows out. The government's response — 75% combined subsidies (50% central, 25% state) for fabs and OSATs — represents unprecedented global support for semiconductor packaging and assembly, which contributes 25% of the value chain.

He provided an overview of India's manufacturing pipeline: ten ISM-approved projects including two wafer fabs and eight OSATs, plus two additional OSATs (RRP Electronics and Kaynes SemiCon) proceeding independently. This total of 12-14 OSAT projects, several already operational, represents tangible progress beyond policy. Mr. Keskar set clear expectations: the session would explore how companies are navigating the transition from plans to production and what support mechanisms could accelerate India's manufacturing maturity.



Mr. Raghu Panicker
CEO, Kaynes SemiCon

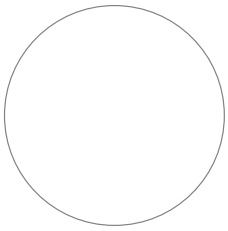
"We should stop saying factories are 'setting up' — they're already set up. Pilot production is happening. It's real now."

Mr. Panicker emphatically corrected the perception that India's semiconductor manufacturing remains aspirational. Kaynes SemiCon's facility in Sanand, Gujarat is operational with pilot production underway, as are facilities by RRP and CG Power. His message was unequivocal: India has moved from planning to execution.

He provided background on Kaynes Technology, a 38-year-old EMS player with revenues around $350 million, now investing $350 million in semiconductor manufacturing. Kaynes SemiCon's approach is structured around six divisions providing complete solutions: Assembly & Test, Reliability & Failure Analysis, R&D (package design), Testing, and supporting services. Alpha & Omega Semiconductor is the first customer, with IPM multi-chip modules in production for Korean customers under a five-year contract. Additional customers include Fujitsu (power domain) and Infineon (silicon microphone localization).

Mr. Panicker described significant investment in test equipment covering digital, analogue, mixed-signal, memory, and RF applications, plus reliability and failure analysis capabilities — capital-intensive services rarely available in India. He detailed partnerships with equipment suppliers and Singapore's Institute of Microelectronics for technology transfer.

Addressing challenges candidly, he described obstacles in securing technology partners (Taiwan-based companies were initially sceptical), talent acquisition (requiring expats from Philippines and leveraging IT services companies' semiconductor divisions), and customer acquisition (overcoming the fundamental question: "Will this really happen?"). He credited strategic partnerships and his board's technology orientation for navigating these hurdles, inviting attendees to visit Sanand to witness operations firsthand.



Ms. Apoorva Raut
CTO, RRP Electronics

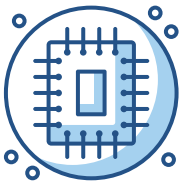
"We are really proud to say we are protecting borders with our surveillance systems — and now we're building the semiconductor capability to sustain them."

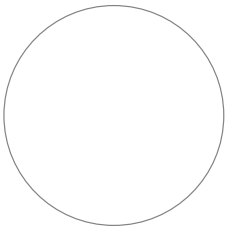
Ms. Raut brought a defence-driven perspective to India's semiconductor story. RRP Electronics emerged from RRP's core defence business manufacturing electro-optical equipment and surveillance systems deployed at India's borders. The semiconductor decision stemmed from strategic necessity: RRP's products depend on thermal detectors imported from Israel and France, creating unacceptable dependencies for defence requirements.

RRP strategically started with packaging operations to build workforce expertise before advancing to fab operations. The company achieved pilot production facility inauguration within six months in 2024. The state government approved two projects: a ₹12,000 crore OSAT facility and a ₹24,000 crore fab facility. By September 2024, the Mahape facility became operational, producing QFN and DFN packages for Taiwan-based partners, with BGA production beginning December 2024.

Ms. Raut outlined RRP's roadmap including compound semiconductor fab development focused on thermal detectors, with a 2027 target for integration into weapons systems. Beyond defence, RRP plans to serve automotive, medical, industrial, and computing sectors with advanced packaging for GPU and AI chips, leveraging partnerships with DECA Technologies. RRP has secured 100 acres in Lote Parshuram MIDC for a power electronics fab focusing on silicon-on-insulator devices, BiCMOS, and silicon photonics.

On challenges, she was frank about customs clearance difficulties with officers unfamiliar with semiconductor materials' urgency — particularly time-sensitive items requiring specific storage. Infrastructure development presented learning curves between pharmaceutical and semiconductor clean room requirements, particularly ESD management. She advocated for customs official education and recognized that until India develops sufficient manufacturing volume, import dependencies on consumables will persist.





Mr. Bing Xue
EVP Global Sales, Alpha & Omega Semiconductor

"We see India's market growing like crazy — and with geopolitical challenges, India offers tremendous supply chain and cost benefits."

Joining remotely, Mr. Xue provided perspective from an established IDM evaluating India as manufacturing partner. Alpha & Omega Semiconductor grew from eight people 25 years ago to 2,000 employees generating $800 million revenue, operating fabs in Oregon and China plus assembly in Shanghai. AOS focuses on power semiconductors and analogue ICs, providing solutions for computing, motor control, battery management, and AI applications.

Regarding the Kaynes partnership, Mr. Xue outlined converging factors: exponential India market growth through 2030, cost and supply chain benefits, and customer requirements for manufacturing diversification beyond China. He emphasized three critical success factors from AOS's journey: entrepreneurial spirit, sustained capital commitment, and talent development over time. His message to Indian manufacturers: AOS succeeded methodically, and with patience, India's semiconductor industry would achieve similar success. The Kaynes partnership represents confidence that India possesses necessary foundations — market growth, policy support, and entrepreneurial determination.

Presentation by Keller

Engineering the Foundations of India's Semiconductor Infrastructure

Dr. Anurag

Dr. Anurag presented Keller's critical but often overlooked role in India's semiconductor ecosystem: providing foundation construction for semiconductor facilities. While most discussions focus on manufacturing processes, Keller addresses the essential infrastructure requirements that enable semiconductor operations.

Keller, established in 1860, is the world's largest foundation solutions provider with operations across 40 countries, 9,000 employees globally, and 2,000+ employees in India over 22 years. The company has executed 400+ contracts across India, developing deep expertise in the country's diverse geology.

Semiconductor facilities present unique construction challenges requiring precision engineering. The Tata Electronics OSAT facility in Dholera, Gujarat—Keller's flagship semiconductor project—demands stringent settlement criteria of just 10mm to maintain operational efficiency of sensitive manufacturing equipment. The project encompasses 170 acres with 60,000+ bored piles, completed within six months using 40+ drilling rigs.

Keller emphasizes that compromised infrastructure directly impacts manufacturing efficiency despite significant investment in equipment and processes. Located in an earthquake-resistant zone near the coast, Dholera requires specialized foundation solutions accounting for seismic activity and soil conditions.

Beyond India, Keller has supported global semiconductor manufacturers including TSMC facilities in Texas and Arizona, bringing international expertise to India's emerging semiconductor infrastructure needs

Panel Discussion 4

Scaling Talent for Chip Design: Academia–Industry Pathways

Panelists:

Mr. Dinanath Kholkar
Professor of Practice, COEP Tech University (Moderator)

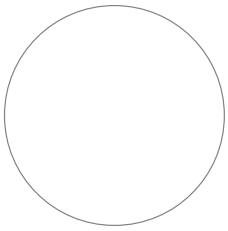
Prof. Maryam Shojaei Baghini
SemiX, IIT Bombay

Mr. Bharat Agarwal
President, Vishwakarma University

Mr. Vivek Pawar
CEO, VidyaLeap i4C

Mr. S D Sudarsan
Executive Director, CDAC

The panel on "Skilling for Scale in Design" addressed the critical challenge of developing talent at scale to support India's semiconductor ambitions. The discussion explored academic initiatives, industry collaboration models, and student engagement strategies necessary for building a skilled workforce. The session was moderated by Mr. Dinanath Kholkar, Professor of Practice, COEP Tech University, and featured Prof. Maryam Shojaei Baghini from IIT Bombay SemiX; Mr. Bharat Agarwal, President, Vishwakarma University; Mr. S D Sudarsan, Executive Director, CDAC; and Mr. Vivek Pawar, CEO, VidyaLeap i4C.

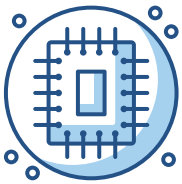


Mr. Dinanath Kholkar
Professor of Practice, COEP Tech University (Moderator)

"We have a Manhattan tower versus a two-story building — that's the gap between IITs and other institutions in semiconductor readiness."

Opening the session, Mr. Kholkar framed the discussion around Pune's aspiration to launch semiconductor clubs across engineering colleges, building on momentum from the SemiX conference. He highlighted a stark reality revealed by recent studies: the capability gap between IIT Bombay and other institutions resembles comparing a Manhattan skyscraper to a two-story building. His recent college visits revealed that even department heads and principals lack awareness of semiconductor initiatives and opportunities, indicating fundamental ecosystem gaps.

Mr. Kholkar emphasized that while 20% of the global semiconductor workforce works in India, very few fabless companies have achieved success from India. He challenged the panel to address practical questions: How can universities build awareness among faculty? What multidisciplinary approaches are needed? How can industry contribute to scaling efforts? His vision centred on creating a network of active semiconductor clubs where students engage with real industry problems rather than academic exercises.



Prof. Maryam Shojaei Baghini
SemiX, IIT Bombay

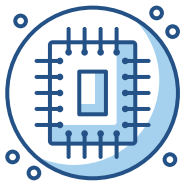
"We need to develop semiconductor thinkers, not just designers — innovation cannot come without fundamental thinking."

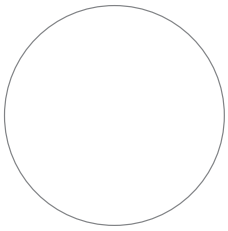
Prof. Baghini presented IIT Bombay's comprehensive approach to semiconductor education scaling through multiple initiatives. SemiX (Semiconductor Excellence), established three years ago and recently approved as an academic centre, operates with extensive industry collaboration defining programs based on industry requirements, internships, and actual needs. The University Affiliate Program, supported by Government of Maharashtra, employs a hub-and-spoke model with IIT Bombay as the hub connecting to multiple institutions across Maharashtra, enabling scalability through regional specialization.

She highlighted the TIDE (Talent for Semiconductor Ecosystem) program led by IIT Bombay under the Ministry of Education, focusing on future technology anticipation, gap identification at international levels, and policy solutions. TIDE operates across multiple verticals including packaging, devices, analogue/mixed-signal design, electronic systems, and materials, providing holistic semiconductor ecosystem coverage.

Prof. Baghini emphasized a critical philosophical shift: moving from service to innovation requires developing fundamental thinkers, not just skilled technicians. Faculty members across academia and industry must nurture fundamental thinking in students because innovation emerges from deep understanding, not rote tool usage. She stressed that scaling must maintain quality, not just increase quantity, leveraging modern technologies and AI-assisted learning while preserving the essential role of teachers in establishing foundational thinking.

The University Outreach Program addresses the practical challenge of reaching beyond elite institutions. She invited faculty from across Maharashtra to participate in pilot programs that will eventually scale nationally, recognizing that semiconductor leadership requires a broad ecosystem beyond a few premier institutions.





Mr. Bharat Agarwal
President, Vishwakarma University

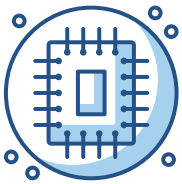
"Electronics departments are experiencing a revival — for the first time in years, students are choosing electronics for domain expertise, not just software jobs."

Mr. Agarwal provided perspective on private universities' semiconductor journey, acknowledging that IITs naturally receive initial research funding and attention in emerging sectors. However, he noted a significant positive shift: electronics departments across Pune and Maharashtra are experiencing revival after years of producing graduates primarily for software industry jobs. The last five years have seen renewed focus on domain expertise and electronics-specific careers.

He described concrete progress at institutions like VIT, with faculty receiving relevant exposure through industry connections and on-campus recruitments motivating students to take semiconductor careers seriously. He cited an example where Lattice Semiconductor initially couldn't recruit from VIT's campus, but after targeted short courses with students, successfully recruited three months later — demonstrating that focused interventions can rapidly bridge skill gaps.

Regarding multidisciplinary requirements, Mr. Agarwal announced VIT's upcoming MOU with COEP for shared laboratory access, enabling VIT students to use COEP's semiconductor facilities. He highlighted growing international academic collaborations, citing VIT's association with IFM Electronics (Germany) for student recruitment and projects, which led to a research lab partnership with Aalen University — demonstrating how industry connections catalyze academic partnerships.

Mr. Agarwal emphasized that academic collaborations are accelerating, particularly internationally where institutions are more open to mutual benefit arrangements. He expressed confidence that the ecosystem will scale through combined growth of companies, government initiatives, and human talent development working synergistically.



Mr. Vivek Pawar
CEO, VidyaLeap i4C

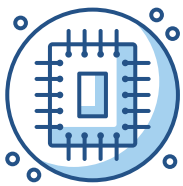
"We need to move from service station to product nation — students must develop product mindset, innovation mindset, and core domain interest."

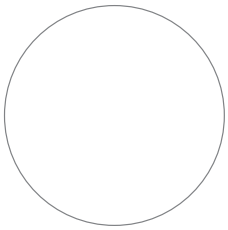
Mr. Pawar, drawing from 20 years at Texas Instruments and subsequent start-up experience, addressed the fundamental challenge of transitioning India from service provider to innovation leader. He shared that VidyaLeap has condensed Texas Instruments' 20-year training model into a five-stage up skilling program, working with colleges nationwide to develop students with product mindset and innovation orientation.

He emphasized three critical requirements for Product Nation aspiration: product mindset (understanding complete lifecycle and ownership), innovation mindset (creative problem-solving rather than following instructions), and core domain interest (genuine passion for electronics rather than using it as pathway to IT jobs). His experience at PVG College demonstrated that when institutions provide openness for industry-embedded models on campus, students in later academic years can receive industry-relevant finishing that dramatically improves employability.

Mr. Pawar challenged the prevailing approach of technology-vertical focused activities (faculty working in isolated areas like cryogenics, plasma, or hydrogen), arguing that real problems require interdisciplinary collaboration. He advocated for faculty members across departments solving common problems together rather than parallel individual research activities with minimal outcome focus.

His key message to students: don't solve trivial or demo problems. Connect with alumni, understand real industry challenges, learn actual tools used professionally, and solve genuine problems. This approach develops skills leading to employment or entrepreneurship. He stressed that student clubs should divide into teams covering chip design, system design using the chip, and testing — ensuring complete lifecycle understanding where learning emerges from discovering and fixing mistakes.





Mr. S D Sudarsan
Executive Director, CDAC

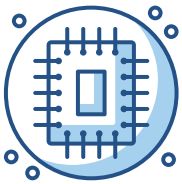
"We started with a target of 350 students five years ago — now we're looking at one chip per student, with 100 chips in the next two years."

Mr. Sudarsan provided comprehensive overview of the Chip to Start-up (C2S) program, which evolved from the modest SMDP (Special Manpower Development Program) targeting 350 students in its first five-year plan to current ambitious scale. C2S focuses on three verticals: infrastructure creation (fabs/OSATs handled directly by government), capacity building through C2S (enabling students to progress from design through post-silicon validation), and Design Linked Incentive supporting established companies.

He detailed C2S's transformative approach to EDA tool access. Rather than forcing institutions into single-vendor lock-in with proprietary tools, C2S created EDA Tool Suite — now the world's largest system offering nine different EDA vendors' tools under one umbrella. This enables 300 academic institutes to access and compare tools, allowing students to determine which tool excels for specific tasks (simulation, timing analysis, and place-and-route), producing better designs and preventing single-vendor dependency.

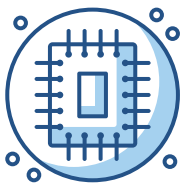
Addressing faculty capability gaps, Mr. Sudarsan acknowledged that only 350 of 600+ institutes offering VLSI courses have applied to C2S, partly because application requires identifying qualified faculty who actually teach relevant courses. Many faculties hold PhDs in the area but have become traditional teachers without industry connection. To bridge this gap, C2S runs Instructional Enhancement Programs (IEP) with EDA vendors, CDAC, and aggregators providing approximately 600 training man-days annually. Five-day residential IAP programs for academic instructors are continuously offered, with eight courses currently running and expansion planned.

He shared remarkable success stories: Last year's Design Hackathon attracted 10,000 students forming 2,500+ teams, with 40 selected for a 100-hour continuous hackathon. Notably, top six prizes included two non-IIT tier-two/tier-three institutions, and one winning team comprised second-year students who hadn't taken any formal VLSI courses but learned independently, competed, and won — demonstrating student capability when provided motivation, visibility, and access to tools.



Mr. Sudarsan outlined scaling initiatives: moving from 100 tape-outs in five years under previous scheme to 100 in one year currently, with a new "One Tape One Student" program targeting 100 chips over two years where every master's student graduates with actual chip fabrication experience. C2S mandates start-up-academic consortium partnerships, providing funding for student-designed chips that start-ups commercialize, bonding entrepreneurship with education.

He emphasized the expanding ecosystem beyond C2S: Samsung challenges, ARM academic programs, state government initiatives (Andhra Pradesh's embedded ecosystem program), Synopsis competitions, and India's own processor development programs (Vega) running parallel challenges.



Valedictory Session

Shaping the Road Ahead: Insights on India's Semiconductor Ecosystem

The valedictory session brought together industry leaders to reflect on the conference's key themes and chart a path forward for India's semiconductor ecosystem. The session synthesized insights from the day's four major pillars: Beyond Fabs, Global Partnerships, Manufacturing Ecosystem, and Skilling for Scale. Speakers included Mr. Ajay Bhagwat, Owner, Renu Electronics; Mr. Ashok Chandak, President, IESA; and Ms. Jaya Panvalkar, Ex-Senior Director, NVIDIA Graphics.

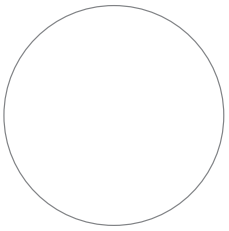
Mr. Ajay Bhagwat
Owner, Renu Electronics (Moderator)

Ms. Jaya Panvalkar
Ex-Senior Director, NVIDIA Graphics

Mr. Ashok Chandak
President, IESA

"Semiconductors have become a buzzword — 3,886 articles published and 180+ TV channels covering the topic in just one month show the momentum we've built."

Mr. Bhagwat opened by contextualizing India's semiconductor moment, noting unprecedented media attention with nearly 4,000 articles and 180+ television channels covering semiconductors in



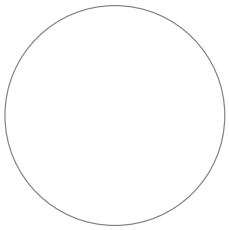
Mr. Ajay Bhagwat
Owner, Renu Electronics
(Moderator)

the past month alone. Even in villages, people now recognize and discuss semiconductors — a remarkable shift indicating genuine national awareness.

He emphasized that the conference addressed not just capital investment (billions in fabs) but the complete ecosystem including design, product creation, and fabless companies. He highlighted that while infrastructure receives attention, India's real challenge and opportunity lies in developing indigenous design capabilities and commercial products. He announced ongoing work to establish a VLSI incubation centre in Pune, with blueprints and approvals in progress.

Addressing self-reliance, Mr. Bhagwat clarified a common misconception: self-reliance in semiconductors doesn't mean isolation or limiting global partnerships. The industry is inherently global, requiring "strategic interdependence" where multiple countries contribute complementary strengths. True self-reliance means controlling critical capabilities while collaborating internationally.

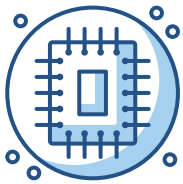
"Maybe 70-80% of our revenues will come from fabless designs — but fabless design is not just a net list, it starts with system design."



Ms. Jaya Panvalkar
Ex-Senior Director, NVIDIA Graphics

Ms. Panvalkar, NVIDIA India's first employee who established the company's Indian operations, provided critical perspective on fabless design requirements. She emphasized that while India may establish a few fabs, keeping them busy requires a robust pipeline of fabless designs — positioning fabless as potentially 70-80% of India's semiconductor revenue opportunity.

She clarified what fabless design actually entails, correcting the misconception that it's merely about EDA tools. True fabless design begins with system design: defining functional requirements, determining hardware-firmware-software partitioning, deciding single versus multi-chip implementations, and selecting IP blocks. Many critical decisions occur before EDA tools are ever used.



Ms. Panvalkar stressed the importance of material science knowledge during fabless design phases. Designers must understand material properties, chip fabrication processes, and advanced packaging techniques including chip stacking. She acknowledged that while India may not immediately compete at

cutting-edge nodes like NVIDIA's advanced products, the goal should be reaching that level eventually. The foundation requires comprehensive understanding spanning system architecture through physical implementation.

Her involvement in the National Supercomputing Mission, where she chairs talent reskilling and up skilling efforts nationwide since 2015 provides perspective on workforce development challenges. She emphasized that scaling talent requires mindset shifts: learning not just tools but underlying principles, applications, quality considerations, and market contexts. Faculty must first genuinely understand new domains before they can effectively teach students.

Regarding high-performance computing and AI, she announced the second National Supercomputing Mission launching January 2026, which installed 37 supercomputers (50 petaflops capacity) for research institutions. Future systems will serve both traditional HPC applications (weather forecasting) and AI applications like autonomous vehicles. She emphasized India's opportunity to develop AI chip solutions and export them globally even before establishing domestic fab capacity — agreeing with targeting achievable wins while maintaining ambition for advanced capabilities.

"We need to think about creating commercially successful chips coming out of India — can I buy a chip designed and manufactured in India for my next-generation product? Today, unfortunately, the answer is no."

Mr. Ashok Chandak
President, IESA

Mr. Chandak framed semiconductor ecosystem development through proven collaboration models, citing MCCI Electronics Cluster Foundation (MECF) as a successful template. MECF addressed a fundamental challenge: over 1,000 Pune electronics companies couldn't access global markets due to lack of testing, verification, and certification infrastructure. Through the Brownfield cluster scheme, industry and government together invested `70 crores (`50 crores government, `20 crores industry) creating world-class facilities for EMI/EMC, environmental, and materials testing.

While the eight-year journey to first customer seemed long, hundreds of SMEs now utilize the facility annually, demonstrating that collective action for common causes works even in Pune's traditionally individualistic business culture. Mr. Chandak proposed applying this proven collaboration model to semiconductors.

He posed a critical question: Can Indian companies design and manufacture commercially successful chips for significant-volume applications like electricity meters, solar inverters, human-machine interfaces, and other products with substantial domestic and export markets? Currently, the answer is no. India lacks brands comparable to NXP, STMicroelectronics, or

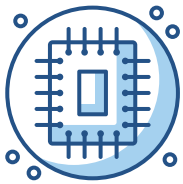
Microchip selling commercial chips globally.

Despite abundant talent (GCCs, design houses, skilled engineers) and manufacturing demand (companies with volume products), the missing element is bringing stakeholders together under one platform. He announced that IESA and MCCI are developing a consortium model, promised to the Ministry of Electronics and IT, to create commercially successful chip ventures spanning 3-5 years.

The consortium would provide: DLI incentive access for companies designing chips for own use or global sales; tool and IP access through CDAC and other partners; and credible platform leveraging MCCI's track record. The vision targets product companies, design houses, and investors working collaboratively with proper program management and risk mitigation.

Mr. Chandak acknowledged entrepreneur hesitation: spending $10 million on chip development without certainty of success creates risk aversion, deterring investment even when economic sense exists. Success stories from experienced companies who've navigated this process must be shared to build confidence. He advocated starting with achievable targets — not 3-nanometer advanced nodes but simpler designs with immediate applications addressing real market needs.

He shared a competitive example: Renu Electronics' large display product competed against Chinese offerings using complete Linux systems with multiple components, while competitors had single-chip solutions integrating everything, enabling $30 price points through innovation, not unfair practices. To compete globally, Indian electronics companies must take similar risks: invest $10 million to generate $100 million businesses. This vision — making Pune and India competitive through indigenous chip development — motivates the consortium initiative.



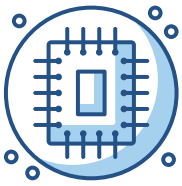
Conclusion

Accelerating India's Semiconductor Mission: Collaboration, Capability, and Scale

The Semiconductor Ecosystem Conference 2025 in Pune marked a defining moment in India's semiconductor journey, demonstrating that the nation has transitioned from aspiration to tangible execution. With India's semiconductor market projected to grow from USD 30 billion to USD 100 billion by 2030, and the electronics industry reaching nearly USD 400 billion, the conference showcased both the scale of opportunity and the comprehensive policy framework supporting this transformation through the India Semiconductor Mission and complementary schemes.

Key themes emerged across deliberations: the urgent need to move beyond service provision toward indigenous product development and IP creation; the critical importance of building complete ecosystems encompassing design, manufacturing, testing, and validation infrastructure; and the necessity of strategic global partnerships that enable technology transfer while maintaining self-reliance in critical capabilities. Speakers emphasized that semiconductor self-reliance doesn't mean isolation but rather strategic interdependence—controlling essential technologies while collaborating internationally.

Maharashtra, particularly Pune, stands at a pivotal juncture. While several manufacturing facilities are operational elsewhere, the state must leverage its strengths in automotive engineering, design talent, and institutional capacity to establish itself as a design hub and manufacturing centre. The conference concluded with concrete proposals including industry-academia consortia for commercial chip development, expansion of training infrastructure through initiatives like C2S and SemiX, and collaborative models proven by MECF applied to semiconductor ecosystem building. Participants recognized that success requires sustained commitment across three pillars: technological development, integrated supply chains, and scaled workforce development—transforming India from a participant to a leader in the global semiconductor value chain.



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